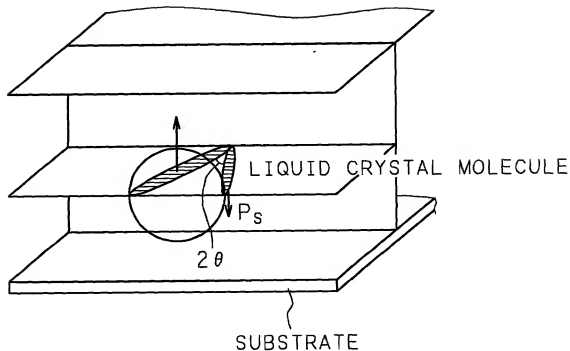
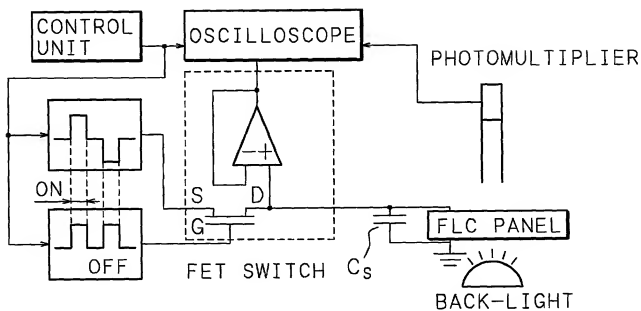


FIG. 1
PRIOR ART



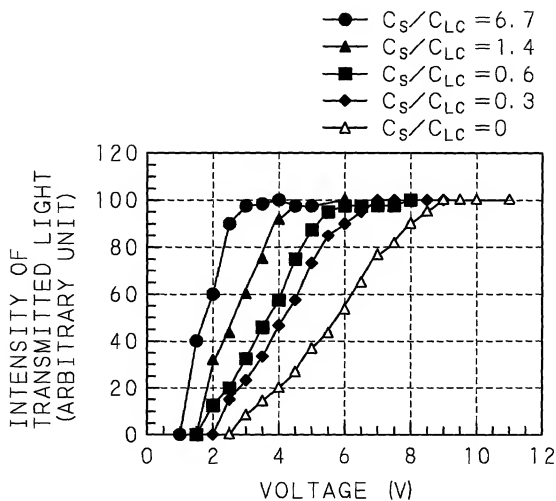
10047732.01502

FIG. 2



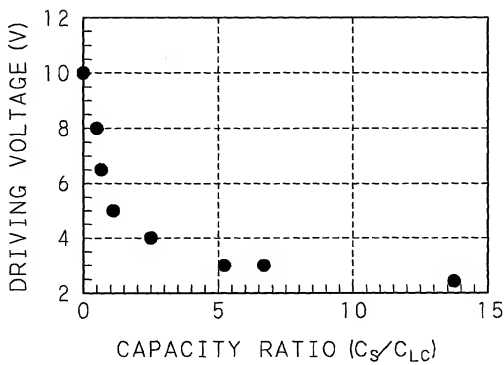
10047732-011502

FIG. 3



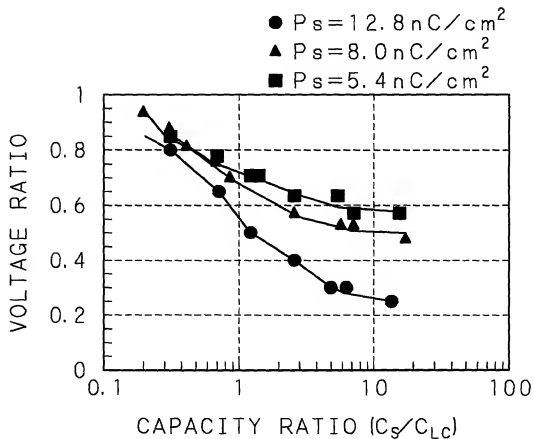
205710.2E74001

FIG. 4



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FIG. 5



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The diagram illustrates the internal circuitry of a video signal processing system. It features several interconnected functional blocks:

- CONTROL SIGNAL GENERATION CIRCUIT (31):** Receives a **SYN** (synchronization) signal and outputs a **CS** (clock signal) to the **REFERENCE VOLTAGE GENERATION CIRCUIT** and a **DCS** (data clock signal) to the **DATA DRIVER** and **SCAN DRIVER**.
- REFERENCE VOLTAGE GENERATION CIRCUIT (34):** Receives the **CS** signal and outputs a **VR1** (reference voltage) signal to the **DATA DRIVER**.
- DATA DRIVER (32):** Receives **VR1** and **DCS** signals, and provides data to the **LIQUID CRYSTAL PANEL (21)**.
- SCAN DRIVER (33):** Receives **DCS** and **VR2** signals, and provides scan signals to the **LIQUID CRYSTAL PANEL (21)**.
- LIQUID CRYSTAL PANEL (21):** The central display element, which also receives **RGBBACK-LIGHT (22)** from the **BACK-LIGHT CONTROL CIRCUIT**.
- BACK-LIGHT CONTROL CIRCUIT (35):** Receives a **PD** (photo detector) signal from the **IMAGE MEMORY** and controls the **RGBBACK-LIGHT (22)**.
- IMAGE MEMORY (30):** Receives a **DD** (data data) signal and outputs a **PD** signal to the **BACK-LIGHT CONTROL CIRCUIT**. It also receives a **DCS** signal from the **CONTROL SIGNAL GENERATION CIRCUIT** via an **AND gate (36)**.

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FIG. 7

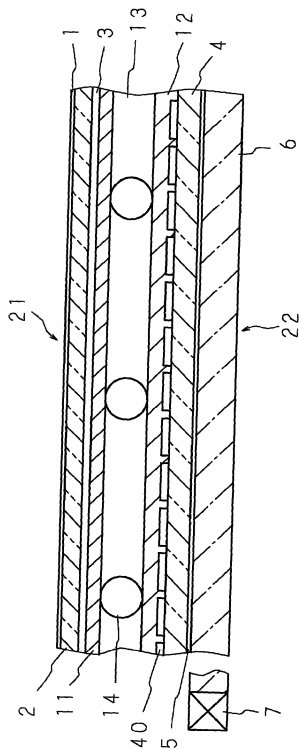


FIG. 8

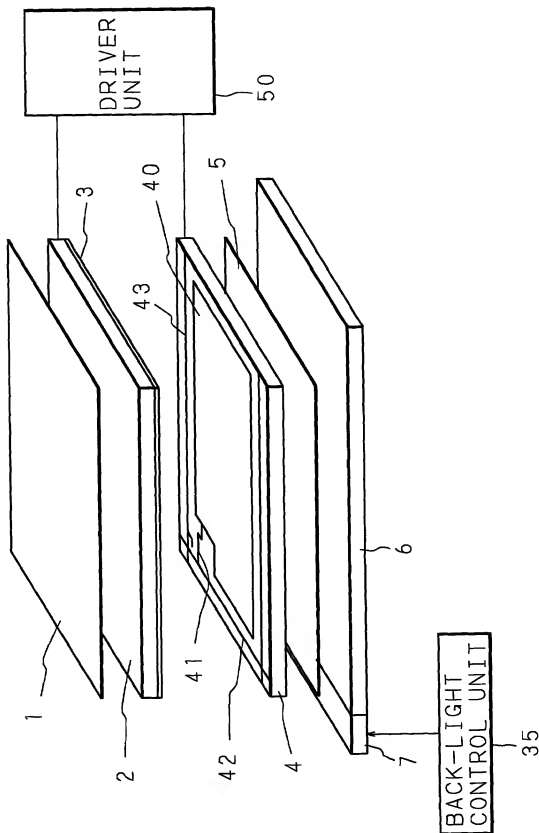
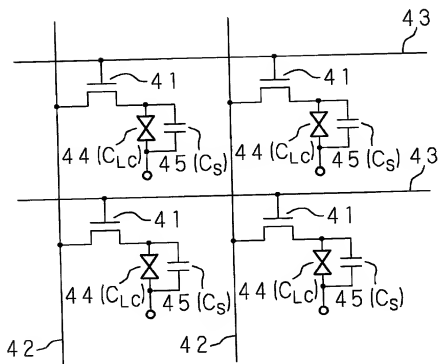
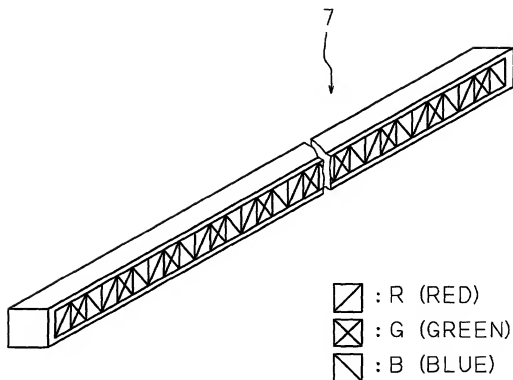


FIG. 9



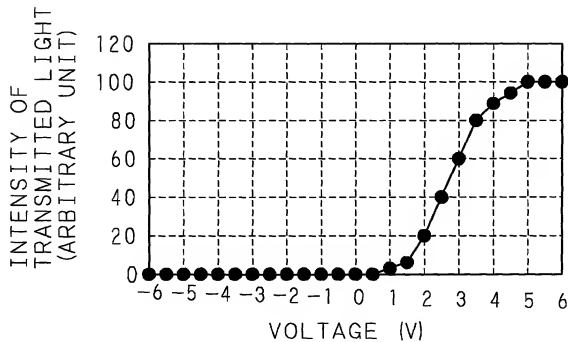
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FIG. 10



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FIG. 11



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FIG. 12

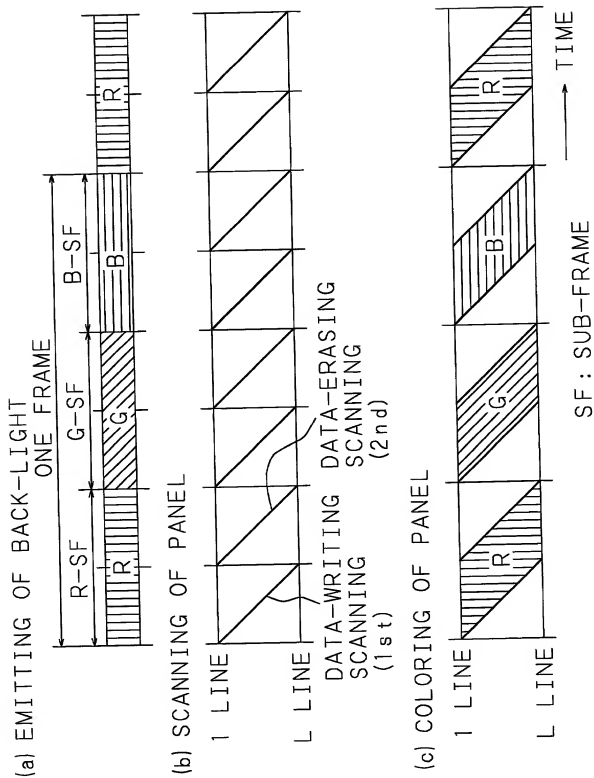
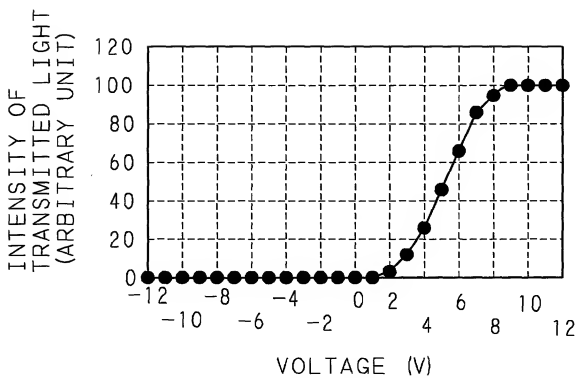


FIG. 13



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